The Analogue Ring Sampler: An ASIC for the Front-End Electronics of the ANTARES Neutrino Telescope.

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On behalf of the ANTARES collaboration

***ABSTRACT*- The ANTARES detector is a 0.1 km^2 scale high-energy neutrino telescope. It will be located in the Mediterranean Sea at a depth of 2400 meters. It consists of a matrix of optical modules each containing a photomultiplier tube. An ASIC named Analogue Ring Sampler has been developed to process photomultiplier tube signals. It measures their arrival time, their charge and samples their shape when this differs from that characteristic of Single Photoelectrons. The digital output is multiplexed and transmitted to the shore through further electronics and an optical link. The main circuit blocks of the ASIC are discussed in this paper.**

1. THE ANTARES TELESCOPE

ANTARES[1] is an undersea neutrino telescope to be deployed at a site located 40 km south of Toulon in France. Its scientific program adresses topics related to particle physics, cosmology and astrophysics.

1.1. Physics goals

Evidence for neutrino masses have already come from neutrino astronomy. The observed flux of electron neutrinos from the Sun is lower than the one expected from the fusion of hydrogen in its core. A similar flux reduction of atmospheric muon neutrinos is observed by Super-Kamiokande. These facts are interpreted as an oscillation of massive neutrinos from one species to another. ANTARES will provide a cross-check of the Super-Kamiokande results by studying the atmospheric muon neutrino flux at a higher energy.

The 70-year old puzzle of the mostly invisible mass of the universe may be solved by neutrino astronomy. If dark matter is composed of weakly interacting massive particles (WIMP) predicted by most versions of supersymmetric theory they accumulate in the core of the Earth, the Sun or at the centre of the Galaxy. Their annihilation yields high-energy neutrinos.

The Sun and supernovae are two confirmed neutrino sources of probably too low energy to be detected by ANTARES. There are numbers of candidate higher energy astrophysical sources which would be detected by ANTARES. Supernovae remnants and microquasars are promising sources within the Galaxy. Active galactic nuclei and gamma ray bursters could be the origin of the high energy cosmic rays detected by air shower arrays. In this case they would produce neutrinos via very energetic proton interactions with the matter surrounding the accelerating engine.

1.2. Detector design

The Earth is a shield against all cosmic rays except neutrinos. The detection of upward-going muons is a unambiguous signature of muon neutrino interactions with the matter below the telescope. A muon is produced at a small angle from the parent neutrino direction and emits Cherenkov light as it passes through sea water. Its trajectory is determined by measuring the arrival time of the Cherenkov light wave front as it propagates through an array of 900 10" diameter photomultiplier tubes (PMT). The array is immersed at 2400 m depth, the top layer of water shielding the detector against most of the downward-going muons produced by the interactions of charged cosmic rays in the upper atmosphere. The PMTs are housed in pressure-resistant glass spheres named optical modules (OM). They are anchored on ten detection lines, each consisting of 30 storeys of three OMs. All the lines are connected to a common junction box and from there to the shore via an electro-optical cable. The large number of detector channels, combined with the single electro-optical link makes power consumption minimization and data compression mandatory. Considering the high reliability needs of an undersea detector and the rather large number of channels, the ANTARES collaboration developed a front-end ASIC, the Analog Ring Sampler (ARS1). The ARS1 is based on two circuits, the ARS0 and the ARS_SPE [2], developed during the R&D phase of ANTARES.

1.3. Performances

The detector is sensitive to neutrinos from about 10 GeV to about 10 PeV with an effective detection area of nearly 20,000 m² at 100 GeV and more than 0.1 km² at 1 PeV. Below 10 GeV the muon track is too short to be correctly measured. Above 10 PeV the Earth is opaque to neutrinos, reducing the angular acceptance to nearly horizontal tracks. It is worth noting that the universe being opaque to photons above 10 TeV, faraway sources can only be visible in neutrinos. The neutrino energy is determined within a factor two to three. The sky coverage is of 3.6π sr with 1.6π sr overlap with the AMANDA[3] neutrino telescope situated at the South pole. The angular resolution

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depends on the physics of the neutrino interaction which dominate at lower energies ($0.7°/[E_\nu/1\ TeV]^{0.6}$) and the time and positioning precision of the detector for the highest energies (0.2°).

2. DATA ACQUISITION SYSTEM

A pair of ARS1 circuits is connected to the output of each optical module via a 2 m long twisted pair cable. The two circuits work in flip-flop mode to minimize dead time. The active ARS1 records any pulse shape coming from the PMT that crosses a user-defined threshold. For time measurements, all ARS1 of the detector are synchronized to a common clock, consisting of a highly accurate and stable 20 MHz signal generated on the shore and distributed throughout the entire detector with offsets calibrated to better than 0.5 ns.

The mode of operation of the front-end data acquisition is based on the discrimination between single photoelectron (SPE) -- when the OM is hit by one photon (or one single bunch of photons)-- and complex (named waveform hereafter) signals -- when several photons hit the OM. This discrimination is done online by the ARS1. In the SPE case, the ARS1 provides a measurement of the charge and arrival time of the photon with respect to the clock. In the waveform case, the ARS1 samples the entire pulse shape. Since SPE pulses amount to about 98% of the events, and generate about 40 times less data than waveforms, this online processing greatly minimizes dead time and dataflow.

The ARS1 chip is designed to measure SPE charges to better than 10% relative precision and SPE arrival times to a precision of the order of 0.5 ns. The anode, the attenuated anode and an earlier stage dynode of the PMT are connected to three channels of the sampler, allowing the recording without saturation of pulses up to 1000 photoelectrons. The fourth channel samples the 20 MHz reference clock used for the synchronization of the whole detector. The four channels are sampled synchronously. The PMT anode is also connected to a threshold comparator, an integrator and a pulse shape discriminator.

The digital data output goes to a DAQ board for storage, multiplexing and transmission to the shore. The circuit is parameterized via a 239 bit scan path serial link. All digital communication signals use differential current logic with a 50 µA differential level to avoid perturbation of analogue signals.

Two additional functions needed for the monitoring of the experiment are implemented on the chip.

3. ARS1 GENERAL DESCRIPTION

The circuit uses 0.8 µm CMOS AMS technology and consists of 68,000 transistors with a total surface of 23 mm^2 (Figure 1).

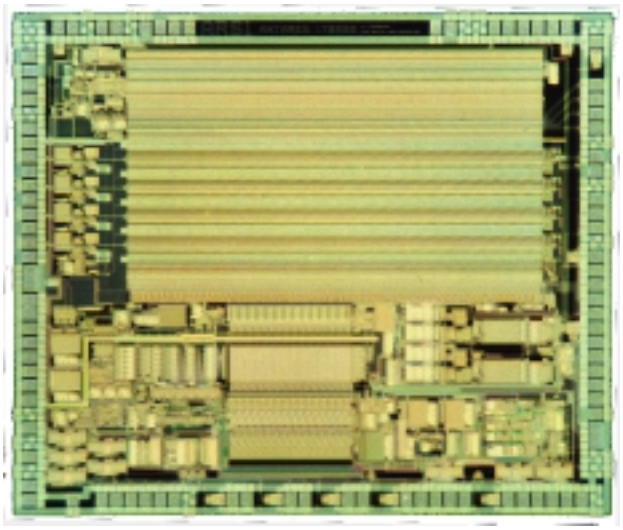

Figure 1: ARS1 Chip in 0.8µm AMS CMOS

It contains 24 DACs for parameter control, two 8-bit ADCs, a pulse shape discriminator, a charge integrator, a time-to-voltage converter, a 16-cell pipeline to store event data and a 4-channel 128-memory cells 1 GHz analogue sampler (Figure 2). All the parameters of the circuit are tunable via a digital port. The data are formatted by an event controller and sent out digitally.

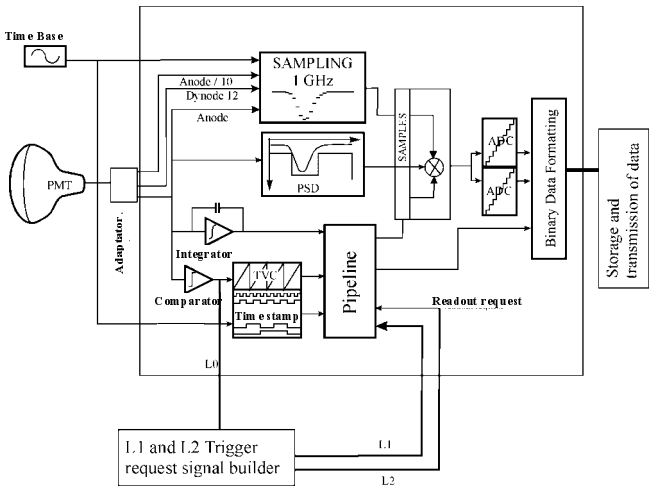

Figure 2: ARS1 architecture

The ARS1 is an asynchronous circuit, driven by the pulse coming from the PMT anode. When the signal crosses the triggering threshold of the comparator, the pulse shape discriminator (PSD) block analyses the shape of the signal and compares it to a predefined template. In parallel the pulse is sampled and its integrated charge is measured. The arrival time of the PMT pulse is given by counting the number of periods of the clock since the last reset (time stamp) and a time to-voltage converter (TVC) block which gives the arrival time within the current period.

At the end of the integration gate, depending on PMT signal shape, the PSD returns a binary result whether the pulse is of SPE or waveform type. In both cases, this information is stored in the 16-memory-cell pipeline, together with the pulse charge, the TVC and time stamp (TS) values.
If the pulse is of the waveform type, sampling keeps running for the 128-sample depth before stopping. Samples are kept in memory awaiting a general readout request. In the chosen architecture, the ARS1 chip can store up to 16 SPE events and one complex waveform pulse in the sampler. Fast sampling being no longer available during the waveform event lifetime data taking is taken over by the second chip.
When a general readout request signal is received within a predefined acceptance window associated with the event, the integrated charge, the TVC value and the waveform samples if needed are digitized by two internal ADCs and sent out serially together with the TS value.

4. FUNCTIONAL DESCRIPTION

In this section the main electronic blocks of ARS1 circuit are detailed.

4.1. Pulse shape discriminator (PSD).

SPE events have a generic shape, and do not need to be digitized. It is only necessary to measure their charge and arrival time. “Waveform” pulses are unpredictable and must be fully digitized. It is the aim of the PSD to decide whether the anode signal is of SPE type or not. Three criteria are used to discriminate these two cases (Figure 3):

(1) Pulse amplitude. A comparator sets a threshold to a pulse level in the range between 2 and 10 photoelectrons.

(2) Time over threshold. The pulse width must be shorter than a duration settable between 10ns and 50ns.

(3) A multiplicity of pulses during the PSD window.

All values of these criteria can be set by slow control via the scan path. The PSD is triggered by the L0 signal and gives its decision in a binary format after the integration gate ends. Depending on the binary result, only charge and time measurements are made for a detected SPE while for “waveform” signals samples are digitized.
When the sampler is in dead time and another waveform type is detected, it is treated as a SPE.

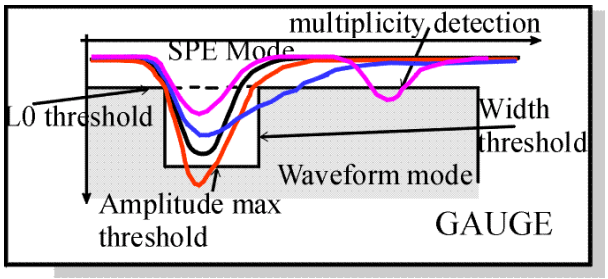

Figure 3: PSD Gauge

4.2. Waveform mode.

Up to four 128-cell channels are sampled at a frequency set between 300 MHz and 1 GHz.
The principle of the fast sampling is based on track and hold cells [4]. A cell in track mode has its internal capacitor connected to the input through a switch. The capacitor voltage follows the input signal until the switch is opened, leaving the cell in hold phase, keeping in memory the input voltage. The sampling frequency is defined by the propagation delay of the hold command between two consecutive storage cells. It is tunable between 1ns and 3ns. The fast sampling runs continuously, connecting the last cell back to the first cell as a ring.
When the PSD has detected a waveform event, it adds this information to the current cell of the pipeline. At the same time, the fast sampling receives a “stop-erasing” signal. The number of cells in hold mode increases until all the 128 cells are in hold mode, stopping the sampling and keeping in memory the input signal shape. The samples can be kept for up to 1 ms before being digitized.

4.3. SPE mode.

The SPE mode consists of measuring the charge and the arrival time of the PMT anode pulse relative to the 20 MHz reference clock.
As the arrival of an anode pulse is random the integration is made by parts. The full charge is the sum of a first integration of the anode signal made before the pulse crossed the L0 threshold and a second integration having a different length. The second integration gate is set by slow control and its duration must be wider than a generic SPE shape.
Until the anode signal crossed the L0 threshold, the first cycle with a predefined period is repeated. During one cycle, three switched capacitors are used for integration: one is in integration, the second is in memorization and the last one is in reset mode. The function of each capacitor changes at each clock cycle as presented in figure 4.

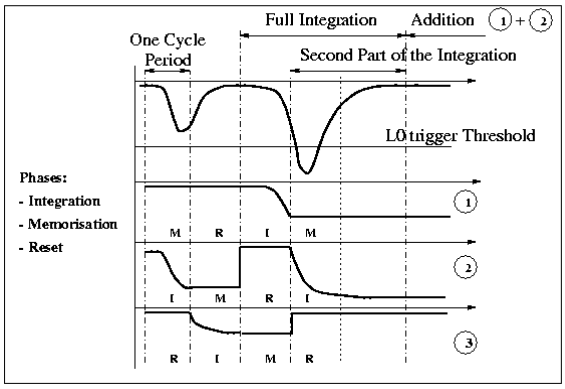

Figure 4: Integration by part.

As soon as the signal crossed the L0 threshold, the current cycle is stopped, replaced by the second integration gate. At the end of the second integration stage, the ARS1 sums the charge on the capacitor in integration mode with that

one on the capacitor in memorization mode. This is the charge value, which will be digitized if needed.
The arrival time is measured in two parts. The time stamp t is a 24 bit counter clocked by the 20 MHz reference clock. A voltage ramp generator is stopped as soon as an anode pulse crosses the L0 threshold. The voltage value is proportional to the phase of the event within the current clock period. The arrival time is found from the time stamp digital value and the analogue TVC value, which will be digitized later on one of the two internal ADC.
An external signal, the Reset Time Stamp (RTS) arrives periodically to reset the time stamp counter to give a time start. Counting each RTS period plus the time stamp value and the TVC value gives an accurate date of the event if it is SPE. Otherwise, we use the shape of the pulse with respect to the digitized reference clock.

The pipeline consists of 16 analogue and digital memory cells to store charge, TVC analogue values, a time stamp value and two bits of information. One bit indicates if the event is of "waveform" type and a second indicates if the sampler contains the waveform shape (Figure 5).

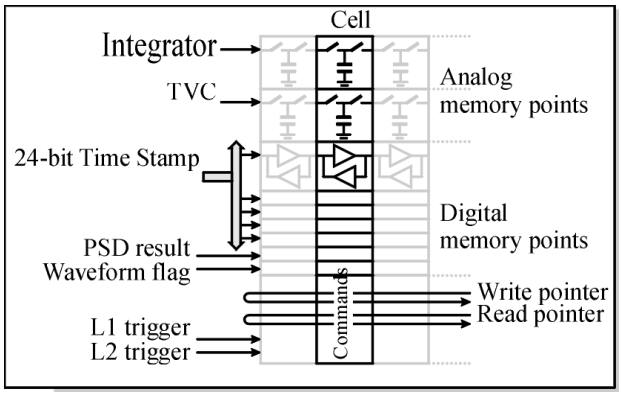

Figure 5: Description of pipeline cells

Thus, the pipeline frees the SPE mode in a few 100 ns, after having written data in a memory cell.
Memory cell values must be stored until a trigger request arrives or until the wait time has ended. Depending on the detector size and the distance between ARS1 and L2 elaboration triggers, the acceptance window of L2 could reach several tens of microseconds. Until the pipeline is full, the ARS1 can accept events into this memory to reduce its dead time.
A write manager, a trigger manager and a read manager control the pipeline. A trigger manager is used to authorize readout requests during the write time. A L1 readout request might follow the L0 signal by only few tens of ns (near coincidence) and must be accepted during the pipeline write phase. L2 readout requests must come later. The acceptance window for L2 trigger must therefore begin after a wait time, which started when the memory cell was written and could end few microseconds later.
The L1 and L2 acceptance window and the L2 waiting time are set by slow control parameters.

4.5. Monitoring and calibration.

A counting rate monitor allows monitoring continuously the trigger rate of each PMT, even in case of very high activity (i.e. bioluminescence in the surrounding sea water inducing rates typically above 1 MHz) when most pulses cannot be processed. In such occurrences, a warning signal is also generated automatically as soon as the event rate reaches a used defined level. The ARS1 also generates electronic pulses synchronous to the clock. The generator provides one or 1024 pulses of at least 50 ns width on the output, determined by a slow control setting. These trigger pulses can be sent to external light calibration devices (LEDs or lasers) for time calibration purposes.

4.6. Readout data.

The ARS1 can send other information besides the SPE and Waveform event data to shore. Each time slow control data is sent, a status event is generated to give the current time stamp value. The previous value of the time stamp counter is sent after the ARS1 received a RTS signal, which reset the counter. The ARS1 can also monitor the event rate and send a counting rate monitor event to the shore, giving the event rate. The ARS1 can manage six types of events shown with their (priority) levels:

1. Counting Rate Monitor event (1)
2. Waveform with the four channels because of saturation.(2)
3. Waveform with only anode and clock reference data. (2)
4. SPE event. (2)
5. Reset Time Stamp event (3)
6. Status event. (4)

As soon as an event is ready to be sent, the read operation consists of connecting the storage capacitor for analogue value to one of the two 8 bit ADC's inputs before going to the digital data formatter.
All data are sent in series on one single output clocked by an external 20 MHz readout clock. Event format consists of a header followed by data .
For analogue data processing, ARS1 has two identical 8-bit ADCs of successive approximation type (Figure 6). Conversion is clocked at 10 MHz, meaning that eight periods are needed to complete a conversion.

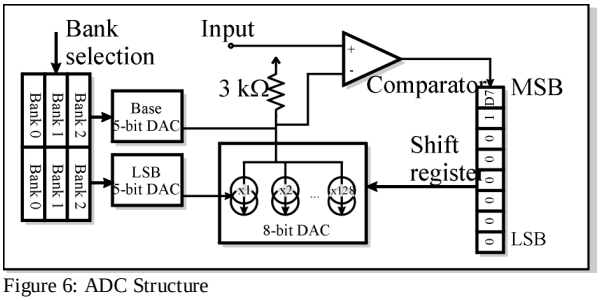

Figure 6: ADC Structure

As six analogue measurements with completely different dynamic ranges have to be digitized in only two ADCs, it is possible to change the LSB value and the maximum convertible voltage of the ADCs. Each ADC has a three-

cell memory bank, each bank filled with the LSB and the maximum ADC amplitude value for one of the six analogue measurements. These parameters are set by slow control (Table 1).

ADC #1	Bank n°1	Anode divided by 5 signal
	Bank n°2	Anode Signal
	Bank n°3	SPE Charge
ADC #2	Bank n°1	Dynode 11 Signal
	Bank n°2	Reference clock
	Bank n°3	SPE TVC

Table 1: Link between ADC banks and data values.

4.7. Miscellaneous functions.

In order to limit the dead time of ARS1 during acquisition, two ARS1 can be daisy chained together. The communication protocol is based on a token, which is transmitted from one ARS1 to the other, working in flip-flop mode. As soon as a L0 trigger signal exists, the ARS1 with the token, will pass the token to the other if it is available for the next event (not in dead time) before making the measurement.

The ARS1 has 75 parameters representing 239 bits. A slow control sequence is initiated each time it is required to program the circuit. It is a serial protocol. A scan path throughout the circuit from one register to another constitutes the slow control architecture. Each register controls DACs. They are 24 of these DAC with 3 to 8 bits inputs . A state machine decodes the slow control frame coming from an external bus common to all ARS1 chips.

Some of the parameters add test functionalities for debugging or disabling some of the functions. For example, one may set a bit to trigger all events without waiting for a L1 or L2 external signal. It is also possible to test the data readout machine, sending out pseudo-events to check the format of the data. The slow control also allows the user to program the configuration of a special pin to spy on various critical internal signals.

5. MEASUREMENTS

5.1. Test bench

Test procedures have been automated through a test board and software for virtual instrument. The test bench consists of several data acquisition cards -- six ports of 8 bits for chip control and data readout, a PC DAC board with 6 channels for DC voltage control and a 2 MHz ADC Board to check analog signals – a programmable pulse generator for PMT emulation and a test board similar to the final system (Figure 7).

An FPGA inside the board controls the ARS1 under test operations and regulates communication to the PC. Data are saved in a FIFO, one for each ARS1. Up to two ARS1 could be chained as foreseen in the telescope electronic system. As the direct current logic is not a standard, an ASIC called ARSCONV has been made to convert DCL to CMOS and CMOS to DCL. It is used to help communication between the FPGA and each ARS1. Because the PC is too slow to do real time measurement directly with an ARS1, the FPGA interfaces the ARS1 circuits and the PC. A *"<command> <data>"* protocol between the FPGA and the PC has been created to set different external ARS1 control signals and to withdraw data from the FIFO to the PC memory. Programming an automated test is to write a sequence of *"<command> <data>"* and to analyze data. We built automated tests this way to measure the TVC transfer function, to study noises on each sampler channels. Thus, the characterization test consists of 20 independent programs (TVC test, charge measurement, Sampler base line study etc…). In the remaining part, results from these tests will be described.

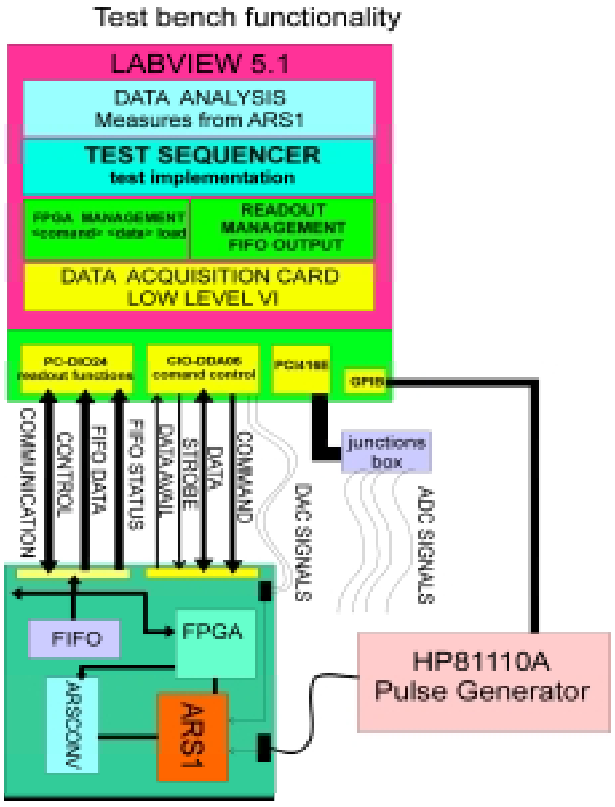

Figure 7: Test bench architecture.

5.2. Preliminary results

5.2.1 Power consumption.

If the ARS1 does not use the input buffer of the sampler channel, the power consumption is less than 200 mW and the two ADCs represent less than 11 mW in the total consumption. Each input buffer adds 30 mW to the final power consumption.

5.2.2 TVC transfer function

The TVC characterization is done by generating a PMT-shaped signal at a tunable time after the reset time stamp

(RTS) pulse. Two successive ramps are made by two independent generators. As the ramps are not perfectly identical, one uses the two first bits of the time stamp counter to know which ramp was used. In real data taking on shore, we can adjust the measurement knowing the imperfection of the ramp. Figure 8 shows the transfer function of the TVC with corresponding time stamp value. The average measured noise corresponds to 800ps jitter on a linearity of 200ps on several ARS1 chips. The noise is twice that expected but it is dominated to external sources. The value remains sufficiently good for the application.

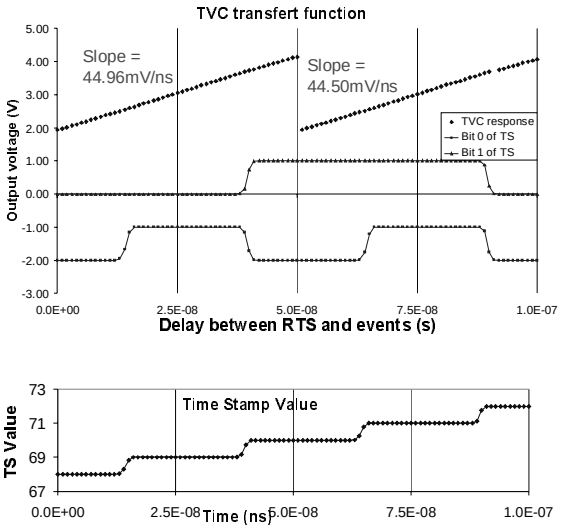

Figure 8: arrival time transfer function of an ARS1.

5.2.3 Integrator test

The Integrator test consists of measuring charge filling the PMT shape signal. Changing charge from a minimum higher than noise to at least 170pC gave us the response of the integrator. For the application, the transfer function slope is set by slow control to 4.5mV/pC (5% fluctuation from one ASIC to an other in figure 9). The integral non-linearity is less than 1% (Figure 10) compared to a 10% specification. Figure 8 displays a typical charge integration response.

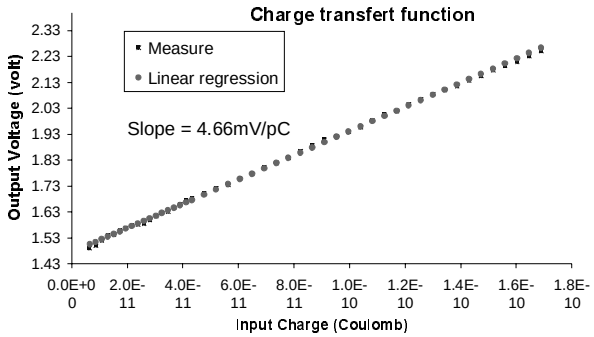

Figure 9: Examples of Charge transfer function

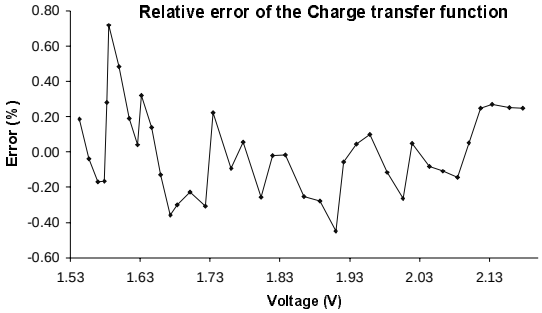

Figure 10: Example of typical relative error of one ARS1

5.2.4 Sampler performances

Figures 11a and 11b show examples of pulse shapes coming from a Hamamatsu 7-81-02 PMT biased at 1300V, together with the reference clock. The ADC LSB is 6mV for the anode signal and 10mV for the sinus signal.

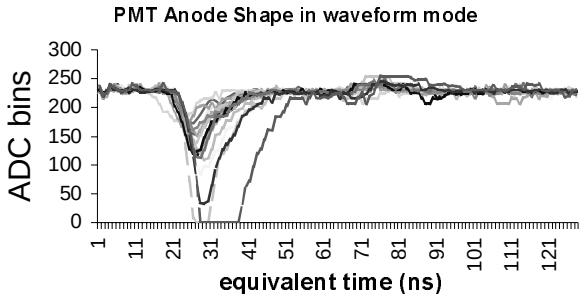

Figure 11a: Examples of anode shape (LSB = 9mV)

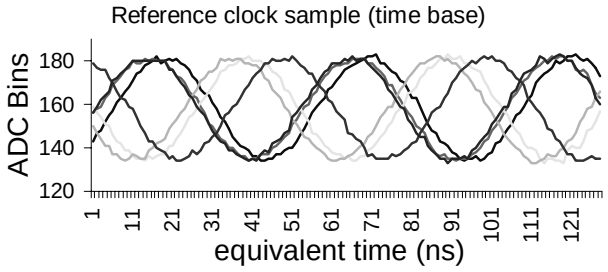

Figure 11b: Examples of reference clock (LSB = 18.9mV)

The base line of the four-channel sampler has been studied. The fixed pattern noise is obtained by taking the average of 250 base line acquisitions; the value is $3mV_{peak}$ (Figure 12). The measured noise, consisting of the noise due to the ASIC plus the test bench noise, is around $5mV_{RMS}$. During the production tests, as part of the calibration of the detector, base line pedestals and noise are systematically measured and kept in the experiment database.

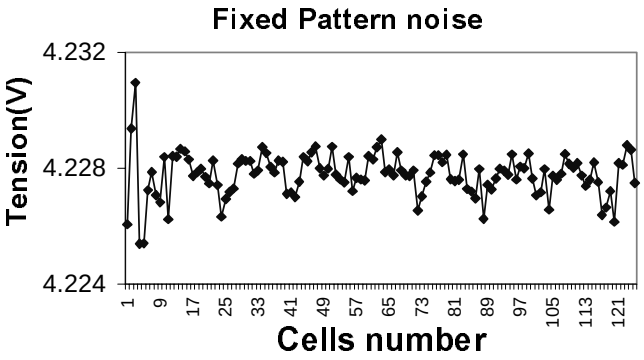

Figure 12: Pattern noise corresponding to the mean of 250 acquisitions.

5.2.5 L1 and L2 trigger test

The test consists of sending 20 events from the pulse generator between two counting rate monitor events. Changing the delay between the L0 signal and the L1 or L2 signal, one counts the number of effective events processed by the ARS1 between the two CRM events. It gave a measurement of the acceptance window for L1 or L2, depending on the used external trigger signal. Figure 13 shows different L2 acceptance windows whose width were changed by slow control. On each edge of the window events are lost because of the internal jitter.

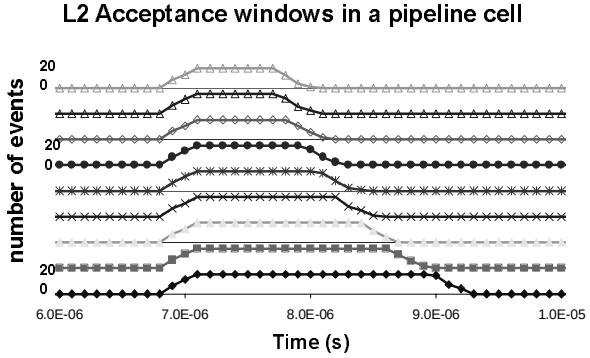

Figure 13: Example of acceptance window measurement.

5.2.6 ADC transfer function

The input of the two internal 8 bits ADCs could be connected directly to a channel of the PC 12 bits DAC board in test mode. Ranging the input DC value from 0V to up to 5V, the ARS1 sent SPE events whose values were the digitization of the DC input. Figure 14 shows example of the ADC response for three different banks of parameters. The graphs display the ADC transfer function of the full scale of the ADC with an LSB equal to 18.9mV and a maximum voltage of 4.87V, of the dynamic range for the charge measurement (LSB=5.75mV; Vmax=2.87V) and of the one for the TVC response (LSB=8.6mV; Vmax=4.495V). Because of the internal 5 bit DAC to convert bank parameters in analogue value, an error of less than 10% has been found. In calibrating each ADC, this error is not a major issue.

The usable range in full scale for the ADC is from 1V to 4.87V. In practice, the ARS1 cannot use the lowest possible scale. The minimum LSB with a correct linearity is 3mV. This value is however lower than the 6mV value specification for the application.

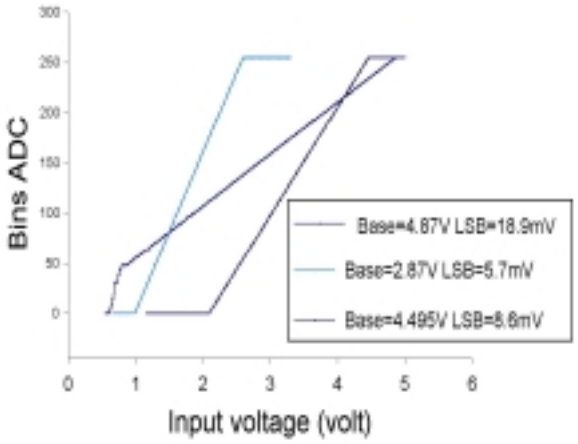

Figure 14: transfer function of 8 bits ADC for four bank of values

5.2.7 Dead time

The ARS1 dead time is the convolution of three independent contributions:

(1) that associated with the TVC and integration measurement. When an ARS1 is processing an event, it cannot process a new event. This dead time depends on the integration gate and on the write time in the pipeline. It is evaluated from 120 ns to 500 ns according to the data set by slow control.

(2) that associated to the sampler. When an event is declared "waveform", the ARS1 stores all the samples until they are read or erased. It takes up to 60 µs to take the decision and 335 µs to sent out data for the 4 channels;

(3) the saturation of the pipeline memory. This depends on the readout clock frequency used to unload the cell information.

Taking into account the observed counting rates at the ANTARES site the total dead time of the detector will be less than 5%.

5.3 Measurement conclusion.

The ARS1 is a low power consumption circuit, adapted to embedded electronics. The environment does not perturb the measurements during the acquisition of events. External trigger signal events managed to validate correctly events. Gathering all the measurement results in a table (Table 2), we conclude that the ARS1 has the right properties for the ANTARES telescope.

Parameters	Measured values
Power consumption	< 200mW (at 5 V)
Sampler frequency	300 MHz to 1.1 GHz
Sampler noise (RMS)	5 mV
Sampler dynamic range	4 V (50 pe)
Waveform mode gain	0.9
Integrator dynamic range	130 pC
Integrator transfer function	4.4 mV/pC
Integrator Integral Linearity	1%
Input bandwidth	130 MHz
Readout clock	10MHz to 25 MHz
TVC transfer function	44.5 mV/ns
TVC Noise (RMS)	800 ps
TVC Integral linearity	200 ps

TABLE 2: ARS1 CHARACTERISTICS

6. CONCLUSIONS AND PROSPECTS

The ARS1 circuit is a result of a long R&D study inside the ANTARES collaboration. In 1996, a first version of the chip, called ARS0, was designed as a general-purpose 5 channels 1 GHz sampler, providing the same functionality as a standard FADC, but at much reduced power consumption and cost. This version of the chip has already been used with success by a couple of other experiments, including the HESS experiment, which is using 10,000 of them.

As was pointed out in this paper, the ARS1 chip does much more than signal sampling. It is a complex circuit, equipped with a wealth of additional functionalities, which make it a data acquisition system in itself. It was designed to match very precisely the requirements of ANTARES front-end electronics, with the ability to make decisions online (to reduce dead time), to buffer the data until validation, etc.

A major asset of the ARS1 remains its very low consumption (less than 200mW under a 5V power supply) relative to the number of the integrated electronic functions. The chip is currently being tested and characterized by the ANTARES collaboration before integration in the prototype line of the detector.

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