

A Low Power Multi-Channel Single Ramp ADC With up to 3.2 GHz Virtual Clock

Eric Delagnes, Dominique Breton, Francis Lugiez, and Reza Rahmanifard

Abstract— During the last decade, ADCs using single ramp architecture have been widely used in integrated circuits dedicated to nuclear science applications. These types of converters are actually very well suited for low power, multi-channel applications. Moreover their wide dynamic range and their very good differential non-linearity are perfectly matched to spectroscopy measurement. Unfortunately, their use is limited by their long conversion time, itself limited by their maximum clock frequency. A new architecture is described in this paper. It permits speeding up the conversion time of the traditional ramp ADC structures by a factor of 32 while keeping a low power consumption. Measurement results on a 4-channel, 12-bit prototype using a 3.2 GHz virtual clock are then presented in detail, showing excellent performances of linearity and noise.

Index Terms— Analog-digital conversion, Time measurement, Delay lock loop, Mixed analog-digital integrated circuits, Front-end electronics, CMOS.

I. INTRODUCTION

THE trend in data acquisition systems for modern physics experiments is to digitize signals closer and closer to the detector. With the very high level of integration achievable with modern submicron technologies, the benefit of integrating inside the same chip the analog front-end, the digitization, and a part of the digital treatment is becoming more and more obvious. Nevertheless, the design of high performances ADCs remains a difficult task. As the nuclear science detector granularity is continuously increasing, and thus the number of channels, the readout circuits are becoming massively multi-channel. For these two reasons, multi-channel integrated ADCs are becoming necessary. Multi-channel lower speed ADCs, associated with demultiplexing structures based on fast analog memories, may also replace a high-speed ADC.

Today, a large spectrum of ADC architectures is available. But, for applications with a large number of channels and a dynamic range higher than 6 bits, flash architectures are excluded by power dissipation and area constraints. Semi-flash or pipelined architecture, at the basis of most of the modern commercial ADCs, are better suited. But they are more

difficult to design, especially if good differential linearity performances are required. Successive approximation architectures are easier to design, but their area may become prohibitive if a large dynamic range and a good linearity are needed.

II. THE SINGLE RAMP ADC ARCHITECTURE AND ITS LIMITATIONS

At last, the single ramp architecture appears to be the easier to design and the most adapted to multi-channel circuits. It has been widely used in front-end ASIC [1, 2, 3] for two decades. Several implementations of this architecture are possible. In the most efficient one, the voltage-to-digital conversion is performed by measuring the time between the start of a voltage ramp and its crossing, detected by a comparator, of the voltage

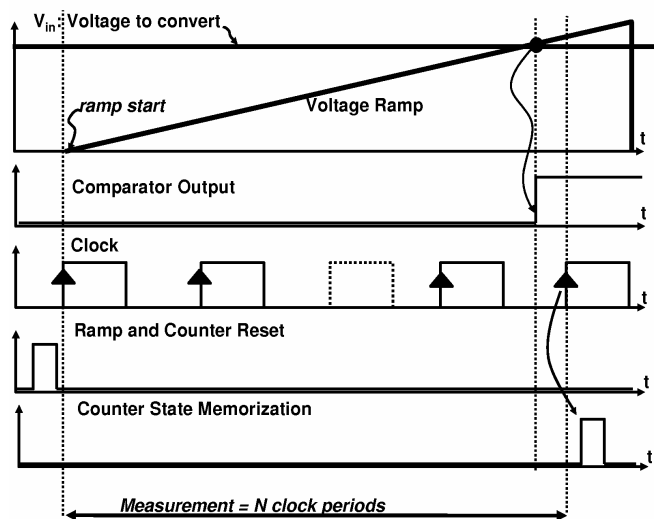


Fig. 1. Chronogram of the standard single ramp ADC operation.

to be converted. Classically, the time measurement is achieved by a counter started synchronously with the ramp as shown on Fig. 1. To avoid metastability effects, a resynchronization of the comparator output by the clock of the counter is required to stop or memorize the counter state. As shown on Fig. 2, the main advantage of this particular implementation is that, the counter and the ramp generator can be shared between the channels so that the ADC part replicated in each channel can be reduced to a comparator and a memory used to copy and memorize the counter state when the discriminator triggers.

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E. Delagnes and F. Lugiez are with CEA, DSM/DAPNIA, CE-Saclay, F-91191 Gif-sur-Yvette Cedex, France (email: eric.delagnes@cea.fr).

D. Breton is with CNRS/LAL, BP34, 91898 Orsay, France.

R. Rahmanifard was with CEA/DSM/DAPNIA during the chip design; he is now with E.A.S.I.L., 124 rue Villaz, 38590 Sillans, France.

Therefore, the power consumption and the area used can be very small even for high dynamic range, and the linearity, mainly dominated by that of the ramp generator, can easily be

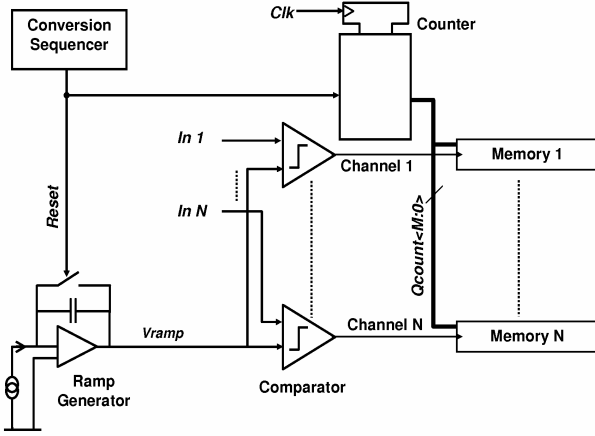


Fig. 2. Possible architecture for a standard multi-channel single ramp-ADC.

very good. But, unfortunately, the use of this kind of ADC is limited by its long conversion time. Actually, for an N bit conversion, it requires $2^N / F_{ck}$, where F_{ck} is the clock

frequency of the counter. So for a 12-bit conversion, making use of a 100 MHz clock, which appears to be a maximum for reasonable power consumption, $40 \mu\text{s}$ are required. This time is prohibitive for a lot of applications.

III. A NEW ARCHITECTURE TO SPEED UP SINGLE RAMP ADCS

A. Global Architecture and Main Design Options

In the new architecture, shown on Fig. 3, as in the usual one, the analog-to-digital conversion is performed by a time measurement, but with a better time resolution. To achieve this, we propose virtually increasing the counter clock frequency. For this purpose, a structure similar to those of modern Time-to-Digital Converters, as those designed for High Energy Physics instrumentation [4, 5], is used to measure the ramping time. As in modern TDC, the most significant bits of the conversion are obtained by a counter operating at moderate F_{ck} frequency while the least significant bits are obtained by an interpolator, making use of a Delay Lock Loop (DLL) with m measurement steps. Many different implementations of this principle are possible; we have chosen one based on the Nutt method also used in [4].

As in the previous ramp based ADC designs, the counter

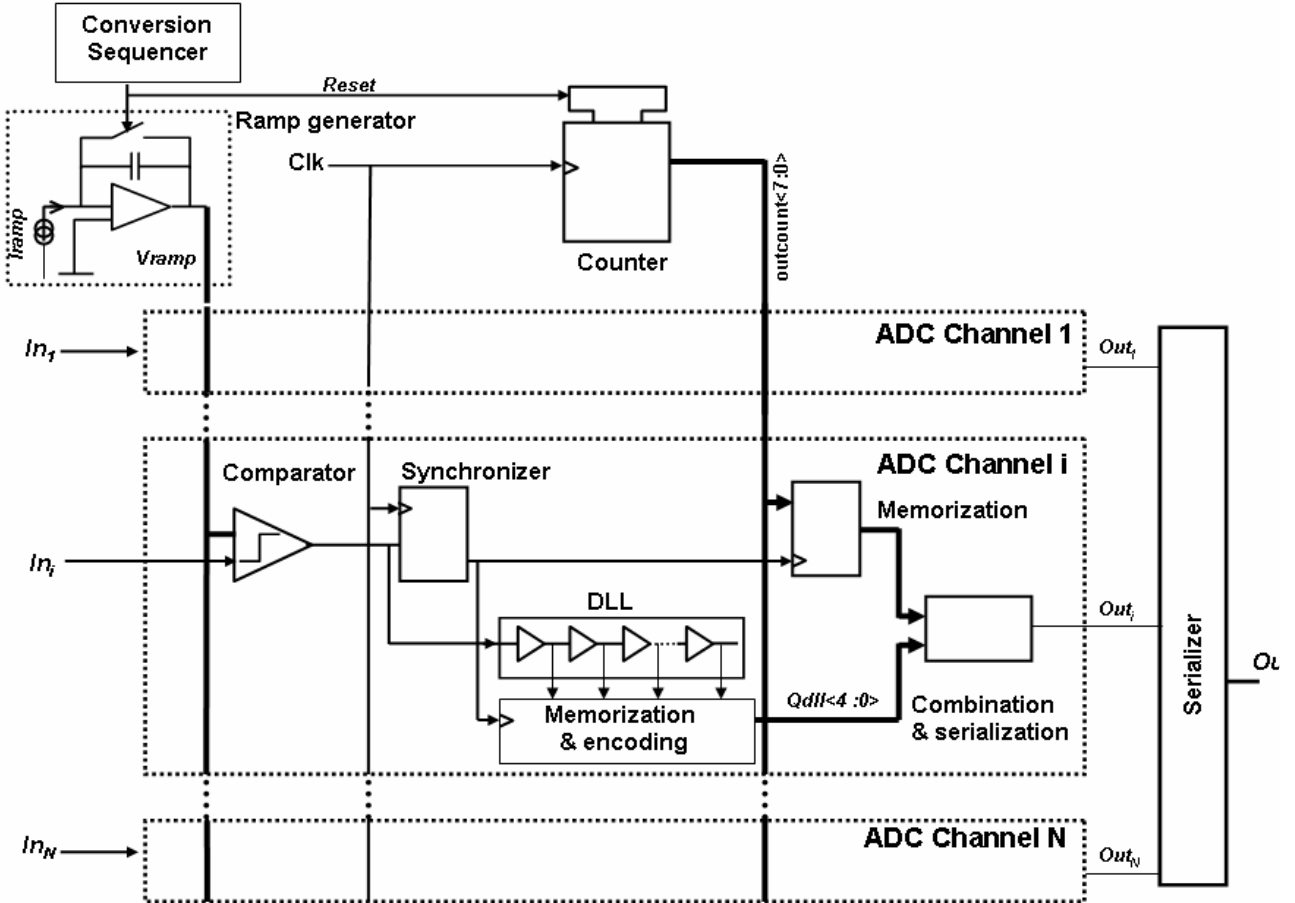


Fig. 3. Block diagram of the improved single ramp multi-channel ADC.

and the ramp are started simultaneously. When the comparator of a channel triggers, its output is synchronized by the clock to memorize the state of the counter. But, in parallel, the asynchronous signal output of the comparator is sent to the input of the DLL. Then the DLL is frozen by the resynchronized comparator signal, so that the DLL memorized state is a measurement, with a $1/(m \cdot F_{ck})$ precision, of the elapsed time between the triggering of the comparator and the next clock edge used to memorize the state of the counter. The DLL and counter output are combined to obtain the ADC output. This interpolation system permits decreasing the ADC conversion time by a factor m while keeping the counter clock frequency, and thus the digital power consumption, unchanged.

B. Main Specifications for a Demonstrator Chip

To validate this architecture, a 4-channel demonstrator, named WILKY, has been designed in the AMS CMOS 0.35 μ m technology. Its specifications were defined to match those of the SAM chip [6] for the H.E.S.S.-II experiment:

- 12-bit dynamic range (and precision) over a 2 V full range: LSB value of 0.5 mV.
- Power consumption < 1 mW per channel.
- Easily extendable up to 64 channels.
- For this design, nominal values of $F_{ck} = 100$ MHz and $m = 32$ have been chosen. Therefore, the LSB time step is 312.5 ps and the maximum conversion time is 1.3 μ s. It corresponds to a virtual frequency of 3.2 GHz.
- Reasonable stability with temperature.

This implies that in the WILKY chip the seven most

significant bits are obtained from the counter whereas the five less significant ones come from the DLL.

IV. DETAILED DESIGN DESCRIPTION

A. The Counter

As in the previous ramp ADC designs [1, 2, 3], the counter is using gray code. In this code, only one bit is changing between two consecutive codes. This minimizes the digital noise and decreases the power consumption of both the counter itself and the digital buffers needed to drive the counter outputs through the channels. This counter is based on a cascade of elementary modular asynchronous blocks. Its depth is programmable from 6 to 10 bits with a nominal value N_c of 7 bits.

B. The Synchronizer

To deal with metastability effects, the discriminator output is re-synchronized by two cascaded RS latches. The first one has its clock input connected to the clock, the second one uses the clock delayed by a string of four elementary delays similar to those used in the DLL and using the same control voltage.

C. The DLL

The total propagation time of the DLL must be larger than the clock period to compensate for the latency of the synchronizer and to deal with edge effects and unexpected delays in the design. For this purpose, as shown on Fig. 4, the DLL consists of $m + p$ elementary delays, of $1/(m \cdot F_{ck})$ each.

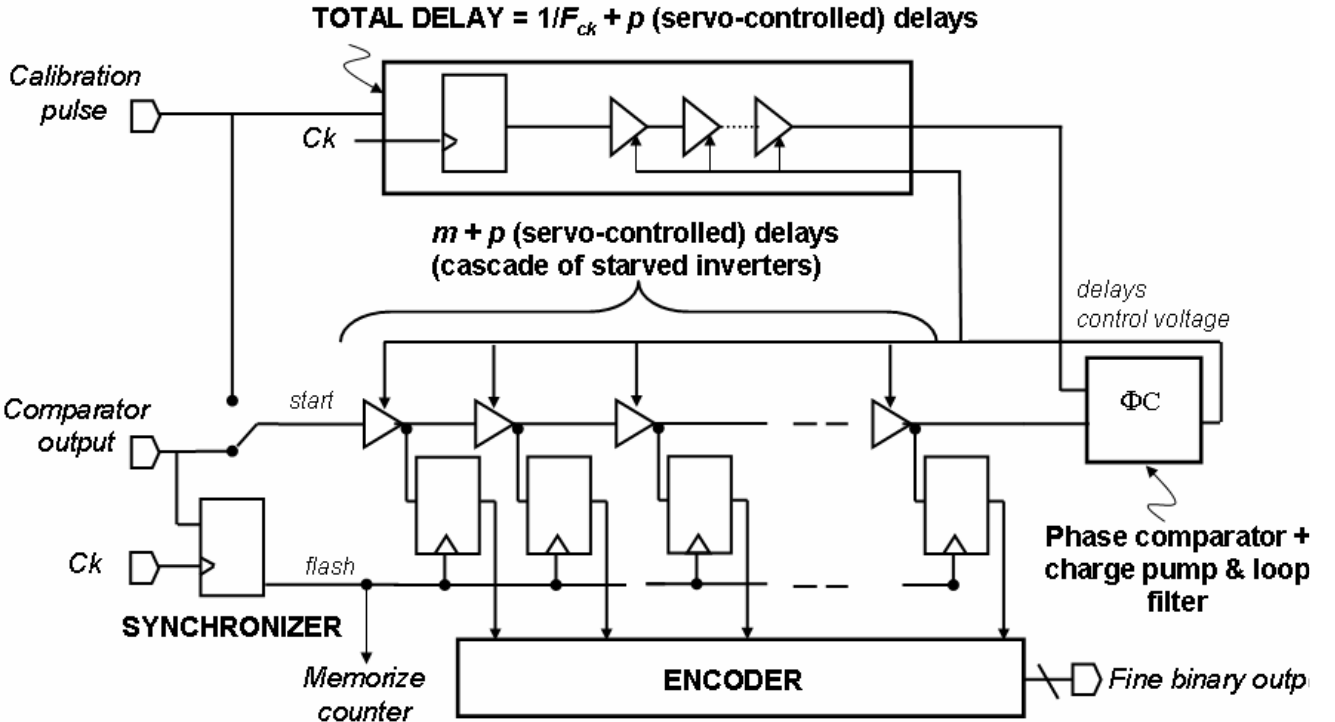


Fig. 4. Block diagram of the DLL and its servo-control loop.

In the WILKY prototype the values $m=32$ and $p=8$ have been chosen. Each DLL elementary delay is the cascade of two starved CMOS inverters. Its speed is voltage-controlled. The states of the DLL outputs are memorized by RS latches, more compact than DFF, when the resynchronized comparator output is triggered.

The main advantage of this architecture including a DLL in each channel is that digital signals are propagating in the DLL only after the comparison is achieved; otherwise the DLL is totally inactive. This minimizes digital activities and therefore power consumption and noise compared to alternative designs with master DLL continuously operating with the clock [5]. But it requires specific calibration phases during which the total delay of each DLL is adjusted to $(m+p)/(m \cdot F_{ck})$ using a servo-control loop. For this purpose, a calibration pulse is sent to the input of the DLL. The phase of the DLL output is compared by a phase comparator with that of the calibration pulse delayed by one clock period (by a DFF) cascaded with p elementary delays identical to those used in the DLL. The output of the phase comparator drives a charge pump providing the feedback voltage controlling the elementary delay value. A minimum of two clock periods is required for this calibration phase, adding extra dead time in the conversion. Practically, at the “cold start” of the ADC operation, only 70 calibration pulses are required to ensure the DLL convergence. Afterward, a $50\mu\text{s}$ calibration periodicity is enough to compensate the charge pump leakages. In the nominal operation, with a 700 kHz repetitive conversion rate, a 2-clock duration calibration phase only is performed only at the beginning of each conversion.

It is expected that the differential non-linearity (D.N.L.) of the DLL will be a non-negligible contributor to the overall ADC non-linearity. For this reason, the length of the DLL has been limited to 40 delays and special care has been put in the DLL layout and especially to the routing of the power supplies.

D. The Ramp Generator

A faster conversion implies a larger sensitivity to the timing parameters of the ramp generator. Both the slope and the offset of the ramp must be stable with temperature. To achieve a good linearity, the ramp generator, shown on Fig. 5, is based on the integration of a constant current by an active integrator. To ensure the required stability with temperature:

--The current source is servo-controlled.

--All the injected charges are minimized or cancelled by use of dummy switches.

--The differential input pair of the integrator operational amplifier is biased with a transconductance stable with temperature, in order to ensure a constant gain-bandwidth product of the OPAMP.

As demonstrated in [7], the rms noise of the voltage ramp scales with the time as:

$$V_n = 1/C_i \cdot (A \cdot t + B \cdot t^2)^{1/2} \quad (1)$$

where C_i is the integration capacitor, and A and B

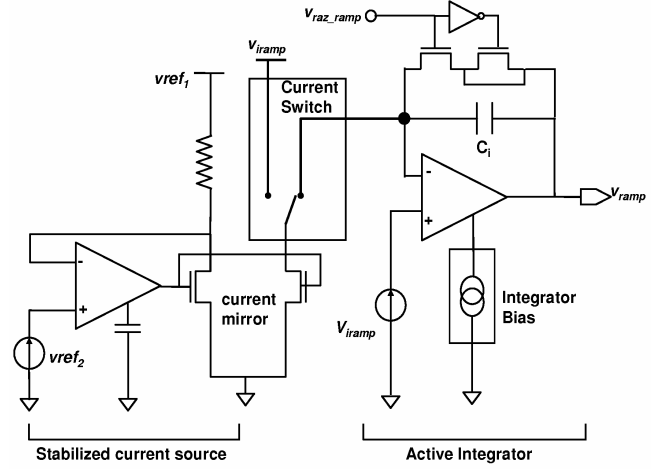


Fig. 5. Principle of the ramp generator common to all the channels.

coefficients related to respectively the thermal and $1/f$ noise contributions of the current source. For a given ramp noise, a faster conversion, like that possible with this design makes it possible to decrease the value of the integration capacitor C_i and then to decrease the size of the ADC. In this design the value of this capacitor is only 5 pF.

E. The Comparator

The fast conversion makes this block really critical. Its delay must be very stable with both the input level and temperature variations. To achieve this, a first solution would be to use a very fast comparator. This solution was eliminated because of its huge power consumption, incompatible with the replication of the comparator in each channel. Instead, a moderate speed, low power structure has been chosen. As shown on Fig. 6, the comparator is based on the cascade of

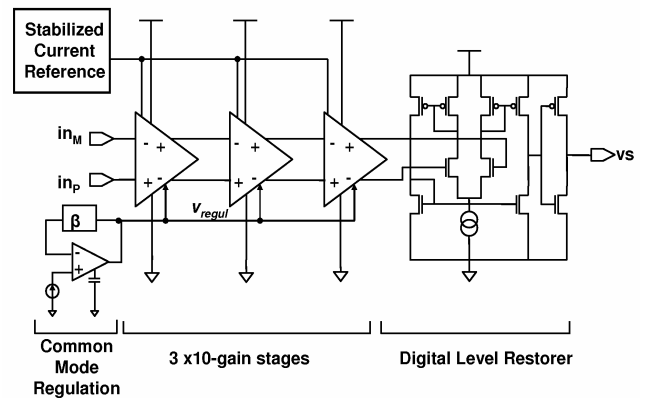


Fig. 6. Principle of the comparator.

three moderate ($\times 10$) gain stages followed by a digital level restorer. Actually, this structure is the one offering the best speed-power trade-off.

The three gain stages of Fig. 7 (right side), are based on simple cascaded differential stages. The cascode pair helps to increase speed and to decrease delay sensitivity to the input

level. For delay stability, they are biased with a temperature-compensated current source. The active loads of these stages consist of MP0 and MP2 PMOS transistors mounted as diodes in parallel with MP1 and MP3 PMOS transistors used as voltage-controlled resistors. This composite load behaves like a resistor for small signals but limits the output swing for larger signals.

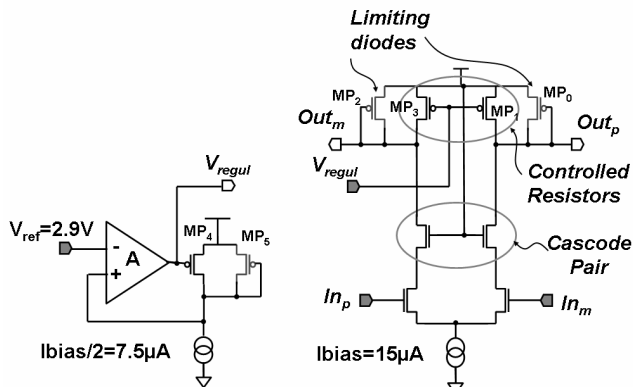


Fig. 7. Replica-based voltage reference (left side) and Gain stage (right stage) used in the comparator.

The delay variations with temperature and technology parameters of the comparator are mainly due to those of the swings and of the output resistance of the gain stages. To minimize these variations, the quiescent output voltages and output swings of each gain stage outputs are carefully controlled by a voltage applied to the gate of MP1 and MP3. This voltage is provided by the reference detailed on Fig. 7 (left side), common to all the channels, in which a replica of a half of the comparator active load biased on its quiescent operating point is put in the feedback loop of an operational amplifier. Thanks to the feedback, the reference voltage provided by the operational amplifier output ensures that the replica output voltage (and therefore the quiescent output voltage of the load) is equal to an external reference voltage independently of temperature and component parameters.

F. Practical Maximum Conversion Rate

The practical conversion time is $(6 + 2 \cdot N_c) / F_{ck}$ where N_c is the number of bits obtained with the counter. The 6 extra clock periods are needed for the following reasons:

- 2 for DLL calibration before conversion.
- 2 after the ramp start to wait for the ramp to enter its very linear region.
- 1 for the comparator output synchronization.
- 1 for DLL encoding.

Therefore, with a 100 MHz clock Frequency, the practical conversion time is then 1.34 μ S, corresponding to a 746 kHz maximum rate.

V. PERFORMANCES OF THE PROTOTYPE CHIP

The *WILKY* chip layout has been optimized for multichannel applications. The common ramp and counter block area is only 300 μ m x 300 μ m whereas the area of each channel is 1 mm x

34 μ m, matching with the pitch of the SAM chip [6]. The depth of the counter, the slope and the offset voltage of the ramp are tunable. This will make it possible to test several operation modes of the ADC.

The ADC prototype has been tested on a USB-2 interfaced board, housing a 16-bit 4-channel DAC with a 75 μ V LSB and differential and integral non-linearities respectively better than ± 2 and ± 4 LSB. This high precision DAC has been used as quasi-static signal generator to characterize the *WILKY* chip.

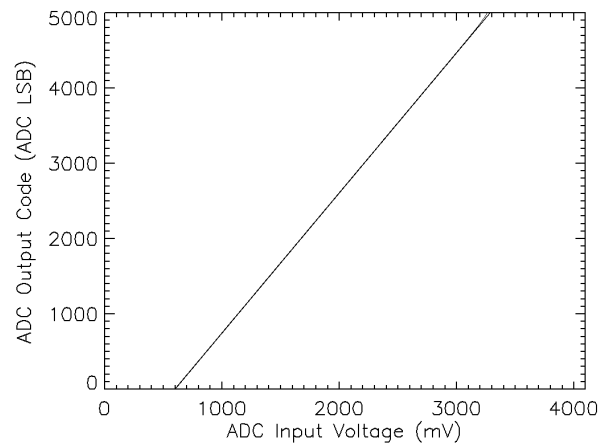


Fig. 8. ADC transfer function in standard mode (data and linear fit superimposed).

A. Tests in the Standard mode of Operation

The prototype has been first tested in its nominal configuration: 12-bit dynamic range, 100 MHz clock.

In this configuration, with a power supply voltage of 3.3 V, the power consumption is only 3.3 mW + 0.5 mW/channel.

The ADC LSB, calculated from the transfer function of Fig. 8 is 534 μ V. It can be noticed that the range of the ADC is

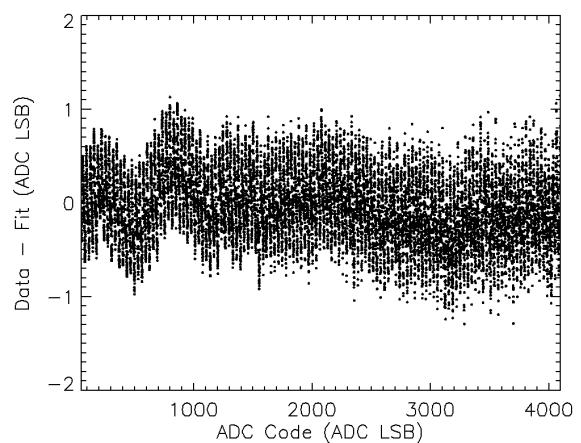


Fig. 9. Integral Non-Linearity as a function of ADC output code.

actually larger than 2V, and that the code delivered by the ADC can be larger than 4096 because the maximum counter depth was set to 8 bits.

The Integral Non-Linearity (INL) plotted on Fig. 9 shows

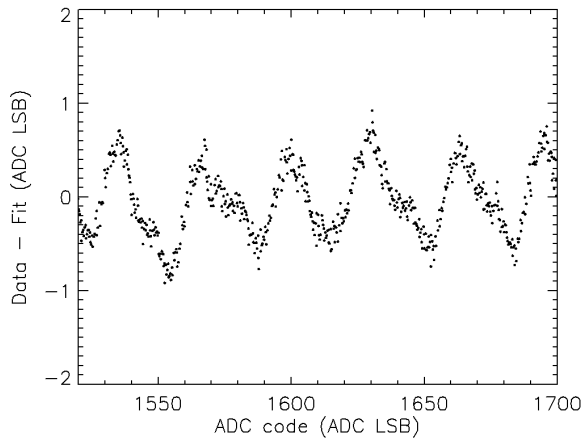


Fig. 10. Integral Non-Linearity: zoom on the Fig. 9 plot.

the residue to a linear fit performed on the data of Fig. 8. The INL is less than ± 1 LSB over the 12-bit range. A zoom of the INL, shown on Fig. 10, reveals a periodicity of 32 ADC counts in the INL characteristic.

For each input voltage of the Fig. 8 transfer function, 512

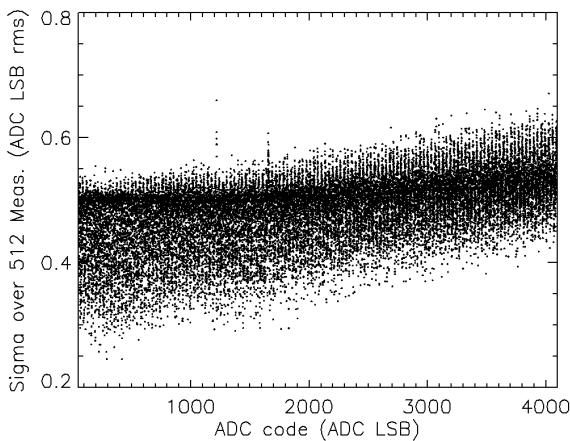


Fig. 11. Variation of measurement variance with ADC output code.

acquisitions have been performed and the noise has been calculated as the variance of these measurements. This variance includes both the contribution of quantization noise and of electronic noise of the ramp generator and the comparator. It is plotted on Fig. 11 as a function of the mean ADC code obtained for each input voltage. The variance remains smaller than 0.6 LSB over the whole ADC range and is increasing with the ADC code as expected from the theoretical noise behavior of the voltage ramp. As for INL, the noise characteristic also reveals a 32 ADC-count periodicity.

The ADC Differential Non-Linearity (DNL) has been characterized using the statistical density of code method assuming a good linearity of the test DAC. On Fig. 12, the normalized density of code is plotted as a function of the ADC code. It is equivalent to $1 + \text{DNL}$. The DNL value is smaller than ± 0.2 LSB peak to peak, or equivalent to 0.1 LSB rms. As for INL and noise, a zoom on the DNL characteristic

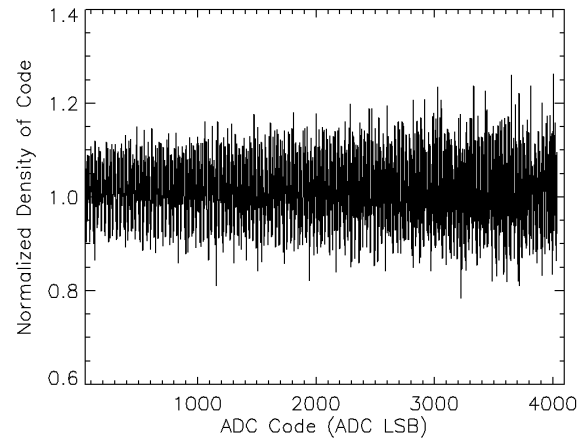


Fig. 12. Normalized statistical density code as a function of ADC output code.

reveals a pattern with a periodicity of 32. This pattern appears to be the major contributor to DNL.

Applying the same statistical density of code method on the same data but using only the 5 bits provided by the ADC permits obtaining the DLL codes probability density plotted on the Fig. 13. The obtained histogram is not flat: some codes are

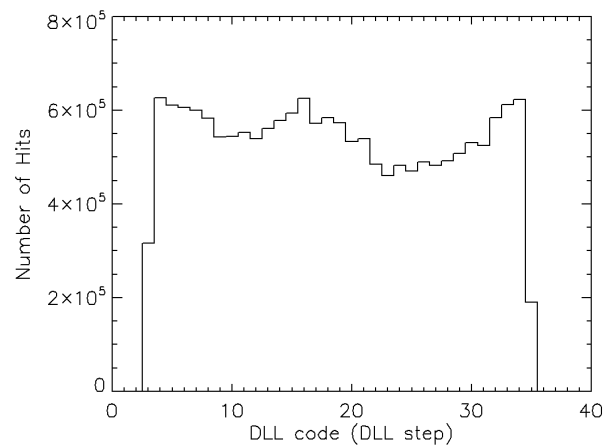


Fig. 13. DLL codes probability density.

more probable than others. It means that the DLL is not perfectly linear. The DNL of the DLL can be estimated to ± 0.15 LSB, corresponding in the time domain to ± 50 ps peak to peak or 20 ps rms. This pattern is the main contributor to the ADC DNL and INL periodicity. It is similar on all the channels and this is probably due to digital couplings inside the DLL.

Even if dominated by the DLL defects, the non-linearity of this ADC remains small and stays comparable to the results reported for standard single ramp ADC chips [1,2,3] with at least ten times larger conversion times.

The measured offset between channels in a WILKY chip is 15 mV peak to peak in good agreement with Monte-Carlo simulations. The spread of transfer function between channels is smaller than $\pm 1/1000$, which is slightly larger than the expected value. There was no measurable crosstalk between

channels.

Fig. 14 demonstrates the good stability of the ADC measurement with time for a fixed input and Fig. 15 its low sensitivity to temperature variations.

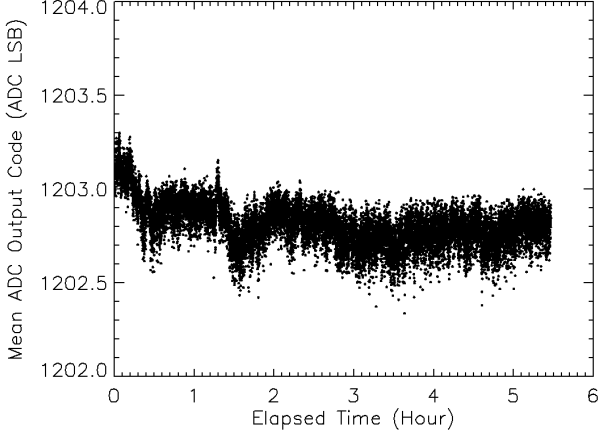


Fig. 14. Stability of the ADC measurement with time. Each plotted dot is the mean value of 512 measurements.

The drift due to temperature is less than 3 LSB in a 10°C range. It is better than our expectation and sufficient for our applications. The shape of the temperature characteristic appears to be identical on all channels.

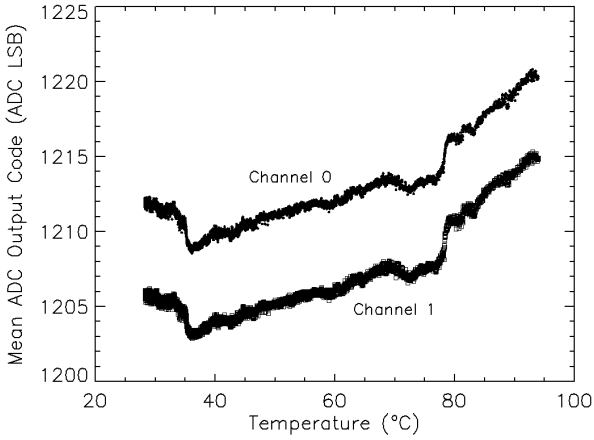


Fig. 15. Variation of the ADC measurements with temperature. Each plotted dot is the mean value of 512 measurements.

The performances of the ADC used in the standard mode are excellent and comparable to those of a genuine 12-bit ADC. If we consider that the prototype is a real 12-bit ADC we can calculate its Figure of Merit (FOM) defined in [8] by

$$FOM = (P / (2^{NBits} \cdot 2 \cdot F_{BW})) \quad (2)$$

where F_{BW} is the ADC Nyquist frequency - we will take equal to conversion frequency divided by 2 for the calculation - and P is the ADC power consumption.

The FOM is equal to 1.2 pJ/conversion in the case of a single channel ADC but is decreased to respectively 0.4 pJ/conversion and 0.2 pJ/conversion in the cases of a 4 or a

32-channel ADC as the power of the common block is shared between the channels. These FOM values are comparable to the one obtained for the best ADCs using deep-submicron technologies. This has to be tempered by the fact that there is no track and hold stage in this ADC as it is designed to be used for or with chips already including peak detectors or track and hold stages.

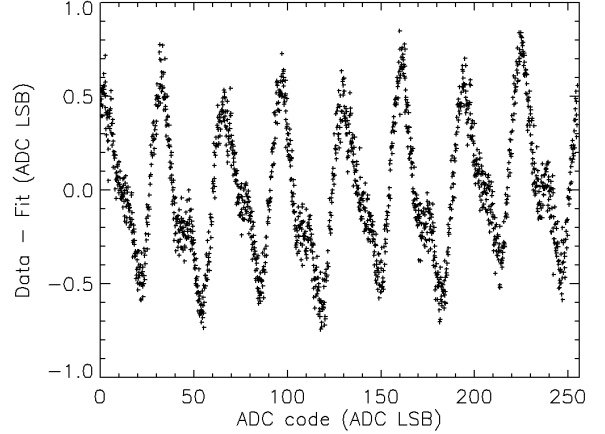


Fig. 16. ADC Integral Non-Linearity as a function of ADC output code in the 8-bit, 1mV-LSB configuration.

B. Tests in Other Conditions

The ADC has also been successfully tested with 25 and 50 MHz master clocks. In these conditions the results are comparable to those obtained at 100 MHz with only a 10 to 20% noise increase for the largest codes due to the largest noise of the longer ramps, as expected from (1).

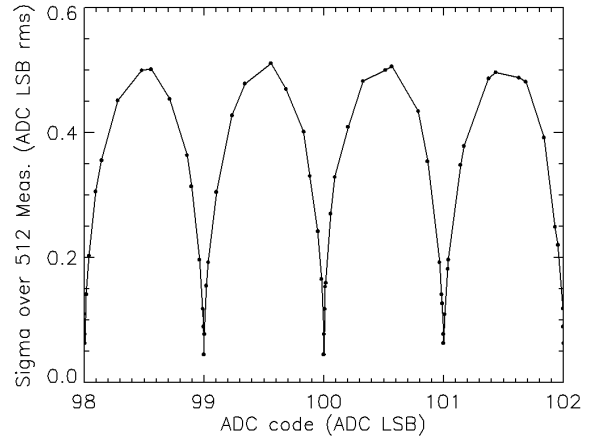


Fig. 17. Zoom on the variance as a function of ADC output code characteristic measured in the 8-bit, 1mV LSB configuration.

A test has also been performed in a configuration in which the ramp slope was increased to obtain a larger LSB value of 1 mV, but with a dynamic range of only 8 bits. Using $F_{ck}=100$ MHz, the maximum conversion time was 140 ns. The INL, measured in these conditions, is plotted in Fig. 16. It is smaller than ± 0.7 LSB, clearly dominated by a modulo-32 pattern. This is again due to the DLL non-linearity contribution which

remains unchanged in this case compared to the nominal one.

The shape of the variance versus mean ADC code characteristic of Fig. 17, measured in this condition, is exactly the one due to quantization effects expected on a low noise ADC: the variance is 0 when the voltage is in the middle of the

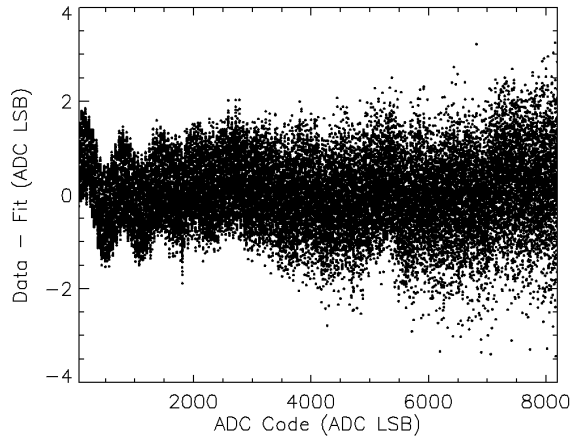


Fig. 18. ADC Integral Non-Linearity as a function of ADC output code in the 13bit, $270\mu\text{V}$ LSB configuration.

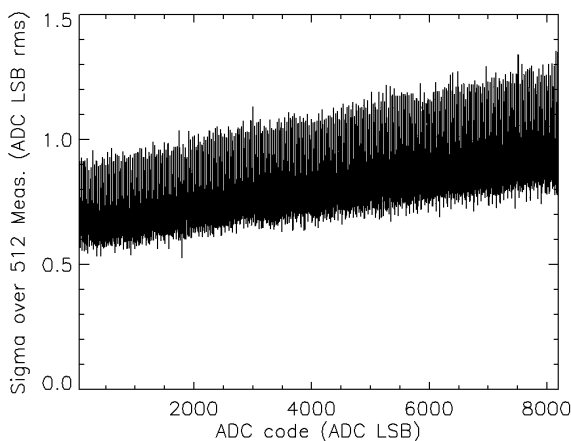


Fig. 19. ADC noise as a function of ADC output code in the 13bit, $270\mu\text{V}$ LSB configuration.

code and is reaching a maximum value of 0.5 when it is near the boundary between two codes. A noise value of 0.15 LSB rms corresponding to the ramp and the comparator noise contributions has been computed from this characteristic.

The chip has also been characterized with a smallest LSB of $270\mu\text{V}$ over a dynamic range of 13 bits corresponding to a longer conversion time of $2.6\mu\text{s}$. In this configuration, the INL, plotted on Fig. 18 is smaller than ± 3 LSB. The noise plotted in Fig. 19 is increasing from 0.7 to 1.2 LSB rms with the ADC code. This is corresponding to almost the same noise voltages as in the standard mode.

According to these results, $270\mu\text{V}$ seems to be the minimal practicable LSB. To be able to use this architecture with a smaller LSB, the noise of the ramp generator at large ramp voltages should be decreased. It can be achieved by increasing

the integrating capacitor C_i of Fig. 5.

VI. CONCLUSION

A new multi-channel single ramp ADC architecture has been proposed, prototyped, and tested. It permits increasing the conversion speed by a factor of 32 without power consumption or other performances penalties. The characterization of the prototype in its nominal 12-bit / $1.34\mu\text{s}$ conversion time configuration has shown excellent performances compatible with a real 12-bit operation together with a good stability. Its differential non-linearity performances make it useful for spectroscopy applications. Considering these excellent results, a 64-channel version of this ADC is going to be integrated on the next generation of a gigahertz analog memory dedicated to the future Cherenkov Telescope Arrays.

Extra measurements, made on other configurations have shown that it is possible to easily adapt this architecture to other applications as long as the LSB remains larger or equal to 0.5 mV. For a smallest LSB, the ramp generator should be re-optimized to reduce the noise. Some other configurations not tested here, such as 5 bits / 100 ns conversion time, where the conversion is achieved by the sole DLL may also be interesting for tracker electronics.

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